Design Methodologies for Heterogeneous Systems and Case Studies of MPSoC Chips

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csem centre suisse d'électronique et de microtechnique

Introduction

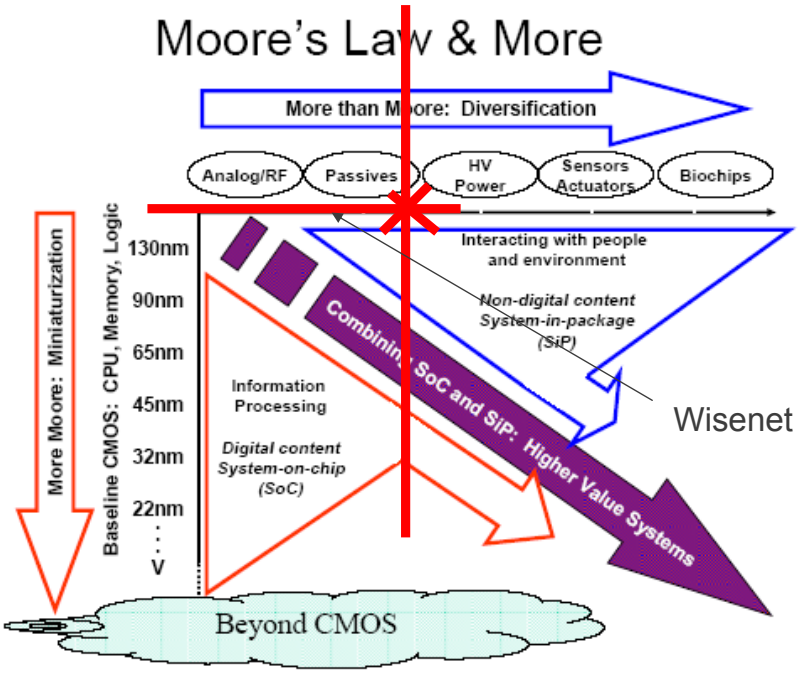
- The design of heterogeneous systems in very deep submicron technologies becomes a very complex task that has to bridge very high level system description to low level consideration due to technology defaults and variations.
- This talk will describe some of these low level main issues, such as dynamic and static power consumption, temperature, technology variations, interconnect, DFM, reliability and yield, and their impact on high-level design, such as the design of multi-Vdd, fault-tolerant, redundant or adaptive chip architectures.
- Some MPSoC chips will be presented in three domains in which heterogeneity is large: wireless sensor networks, vision sensors and mobile TV.

1. What is different today?

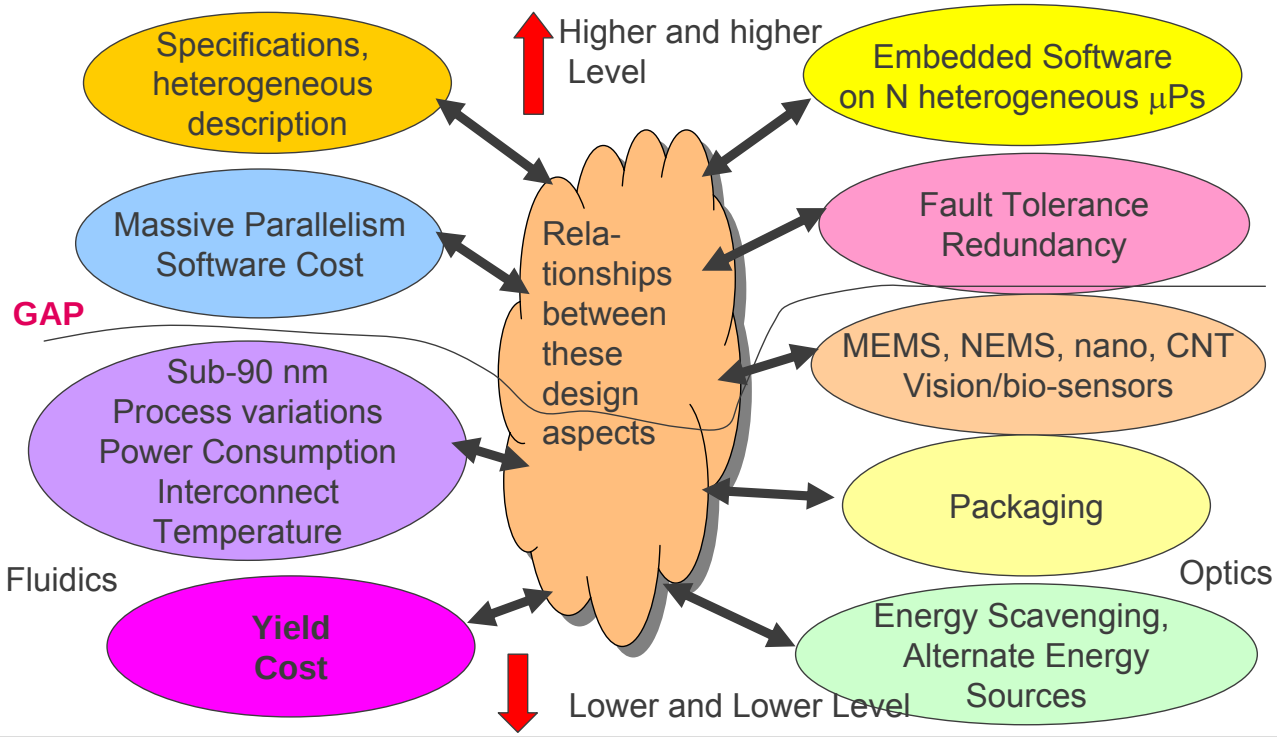
- More Moore
- More than Moore
- Beyond CMOS

- And it is mandatory to simulate and verify everything

It is the famous diagram that everybody knows quite well
What does it mean, practically?

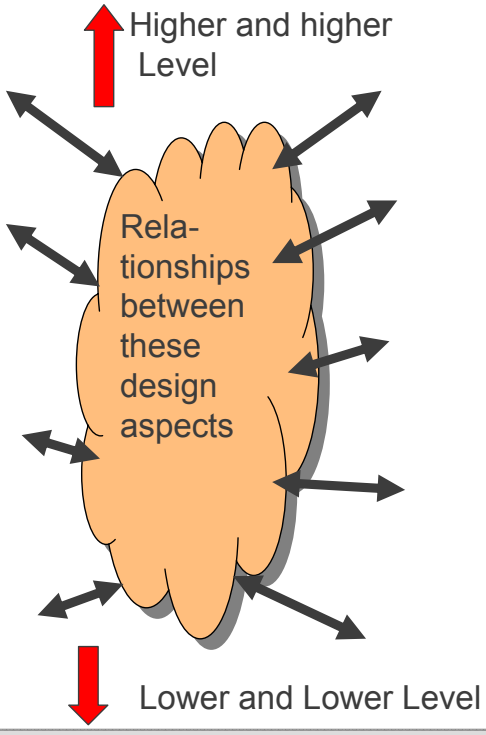


A very long list of problems… very complex…



Why it is so complex…

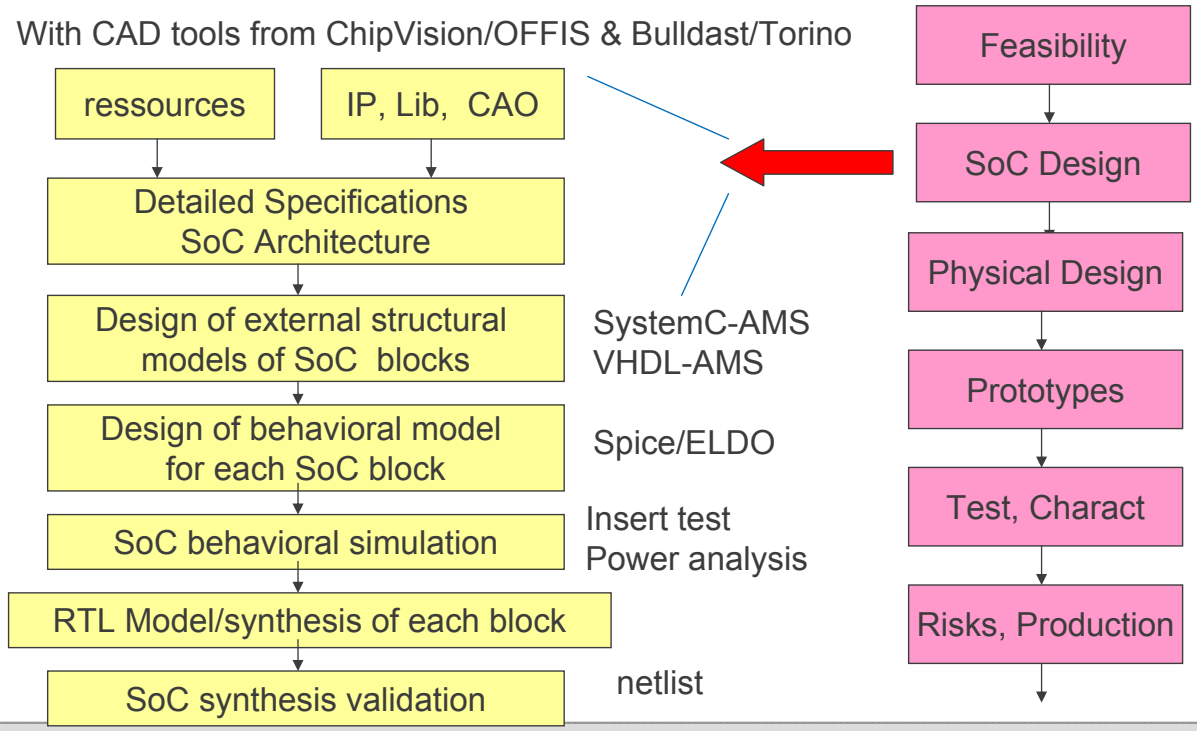
- The relationships between these design aspects are very complex
- **It is extremely interdisciplinary**
- We are going higher and higher, it is ARTEMIS
- We are going lower and lower, it is ENIAC
- With a huge gap between the two, that is larger and larger!!



Citations

- **Ref 1** (T. Henzinger, J. Sifakis) **:**
  - « Computer science research has largely ignored embedded systems, using abstractions that actually remove physical constraints from consideration"
  - "An embedded system is a engineering artifact involving computation that is subject to physical constraints"
    - Control theory: reaction constraints (deadlines, throughput)
    - Computer engineering: execution constraints (power, speed, failures)
  - "The lack of adequately trained bicultural engineers causes inefficiencies in industry"

2. Project FP6 MAP2: CSEM Mixed Design Flow



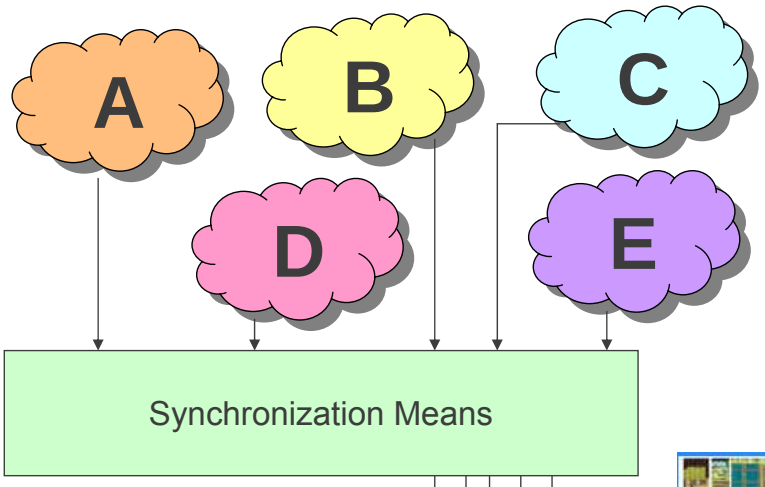
Specifications and System Description

- **Heterogeneous SoC** description at high level:
  - Embedded software
  - Digital processing and amount of memories
  - Peripheral circuits description, a set of very diverse functions, sensors, actuators
- Main Issue: to describe everything in an **unique parallel language**, which will be the SoC specification, and also the behavioral simulation
- What is important:
  - synchronization mechanism of all these processes
  - SoC architecture, what has to be designed (VHDL, analog) and what is already available (existing IP and models)

Questions ?

- Do we have this unique parallel language?
- If yes, is this language very well-known and used by everybody?
- MATLAB, SystemC-AMS ???
- Is such an approach used by a multidisciplinary team, i.e. an unique language used by software people distributing a task on several processors as well as used by people working at low level searching to reduce leakage power of a hardware block?

3. Embedded Software on heterogeneous processors

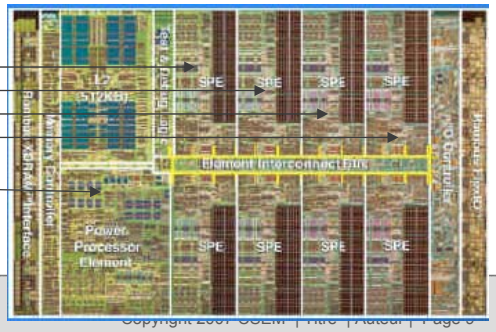


Independent & parallel processes

Mapped on different processors and also on identical processors

MPSoC: application dependent mapping

For identical multicores:
- Parallel compilers, each SPE accepts several processes that are executed sequentially



IBM CELL processor

Embedded Software Mapping onto N cores

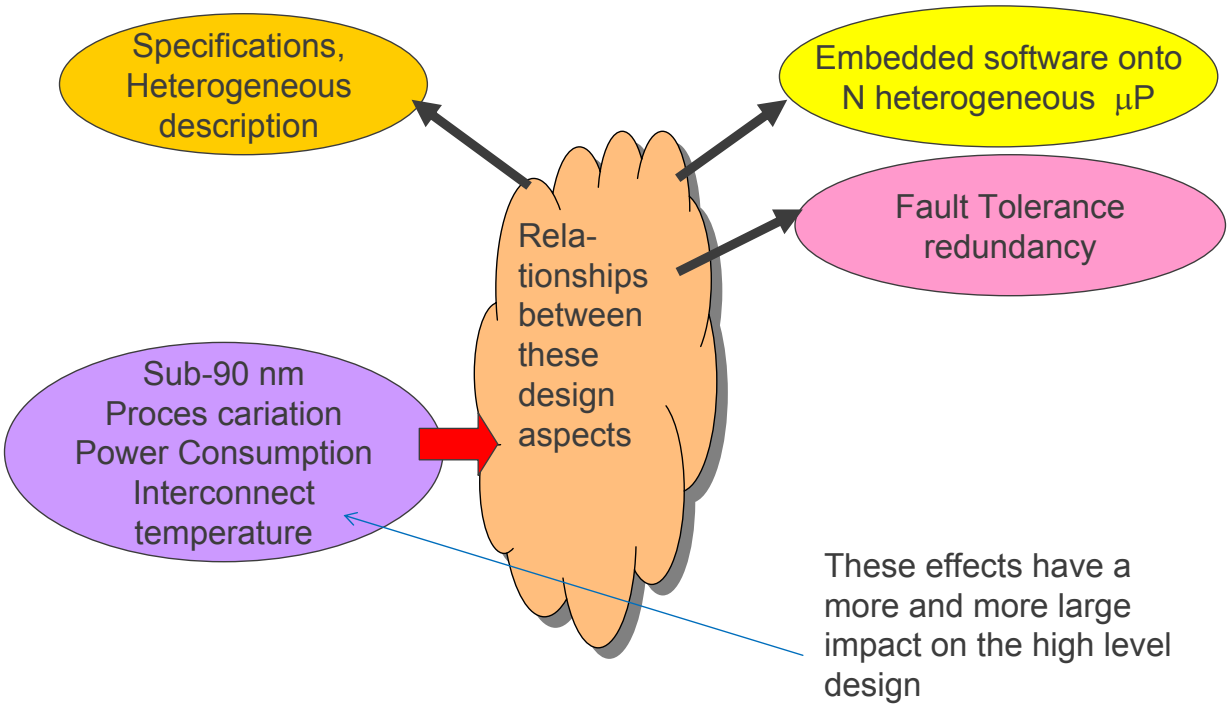
- **MPSoCs:** one has multicores with both different cores (microcontrollers, DSP cores, video processors, co-processors) and identical cores (several identical DSP cores to get enough computation power).
- **The mapping** of the embedded software onto the different cores is dependent on the application and it is generally naturally performed manually
- **Method** like Task Concurrent Management (TCM) has been proposed by IMEC to map tasks in real time MPSoC systems
- **Energy Aware:** Distributing software on to a fixed number N of identical processors is not the best in terms of energy; using dynamically more or less processors depending on the computation load is much better for saving energy.

4. Interdependency from low level towards high level

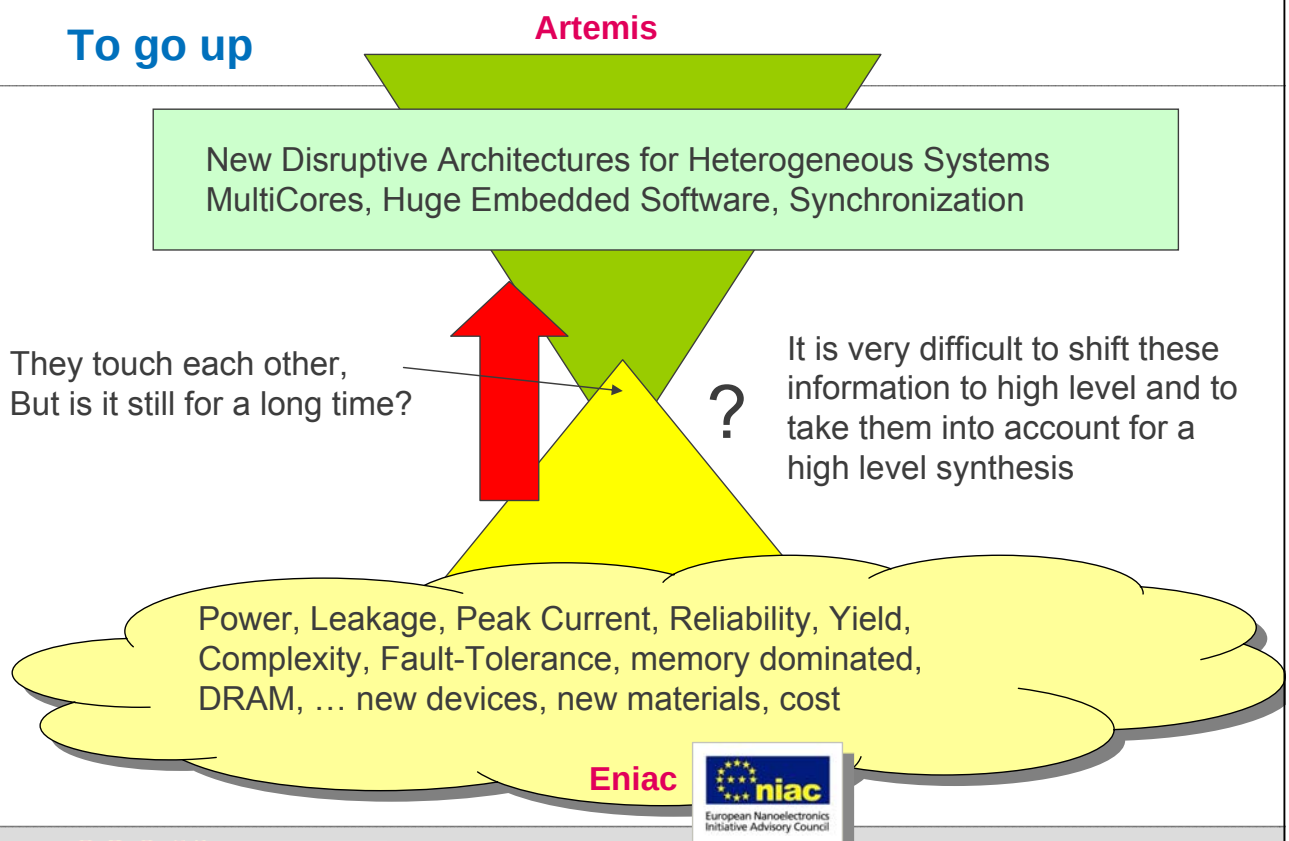
- The problems that we have at low level:
  - Dynamic power consumption, current peak
  - Static power consumption, various types of leakage
  - Temperature
  - Technology variations
  - Interconnect delays
  - Reliability and Yield
  - CMOS « end of scaling » around 11 nm, 2015? « beyond CMOS » (CNT, molecular)

- And we have to shift all these effects to high level to be capable of designing heterogeneous systems that take into account these effects. **What is the impact on the design of architectures?**

To shift these sub 65 nm effects to high level design

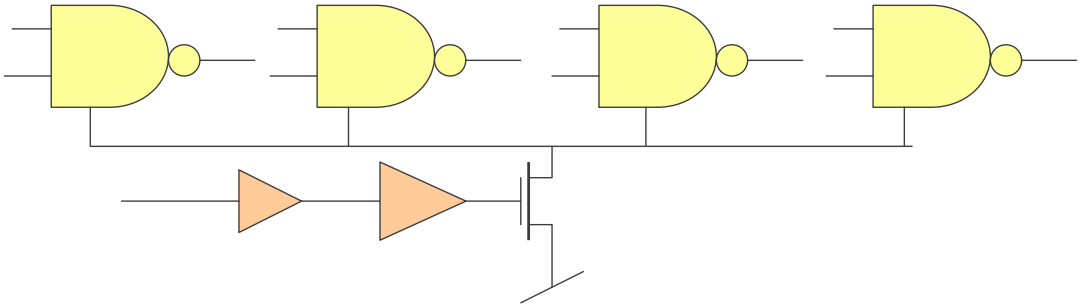


To go up



Example 1: Leakage, impact on architectures

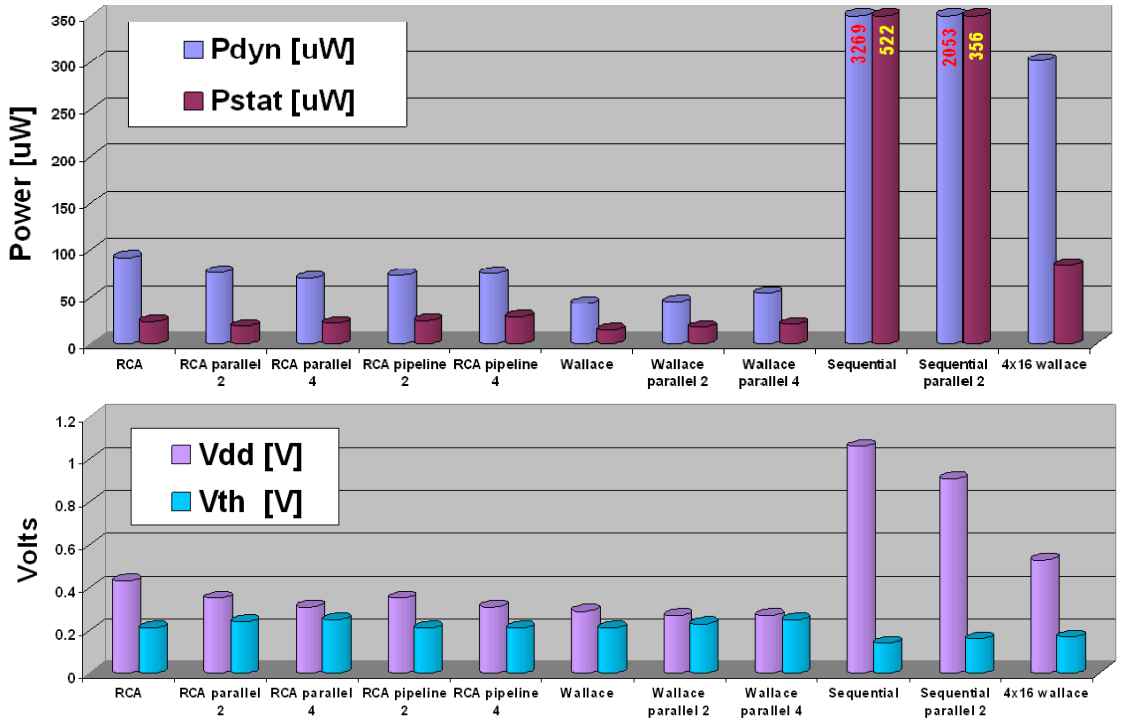
- Leakage current (MOS, CNT, nanowires,..) when they are off, leakage exponential increase with VT decrease, 50% of total power is leakage
- There are many techniques at low or at circuit level for reducing leakage. A well–known and used technique is to have sleep transistors (see Figure below) to cut the supply voltage to idle blocks, but other techniques are also available (several VT, substrate bias for modifying VT, …)



But also at architectural level

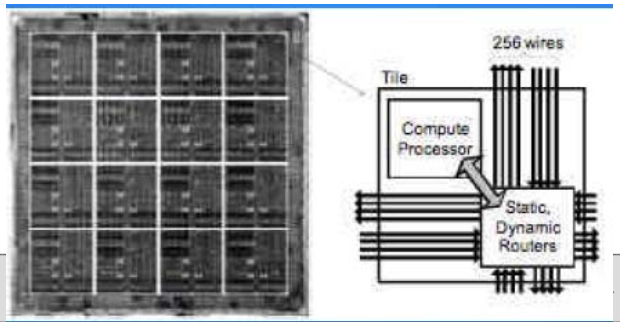
- The basic idea is to ask ourselves if it is possible to find an architecture, for the same logic function, that provides a lower leakage, or a lower total power (dynamic + static) at the same speed
- One searches for an optimal total power considering that the two parameters Vdd and VT are free
- Consequently, a too sequential architecture will present a high Vdd and a small VT to reach the required speed (and a very large dynamic as well as a very large static power).
- Similarly, if the selected architecture presents a too large parallelism, the number of transistors will so large that leakage and total power will be too large
- Example with a 16*16 bit multiplier

11 architectures of multipliers



Example 2: Interconnect delays

- Quite obvious: for every technology reduction factor S, wire delay is increased by a factor S^2!!
- It is a severe problem for busses, but it is a extremely dramatic problem for clock distribution.
- Consequently, the influence on architectures is large: 1) everything could be clockless or asynchronous, or 2) GALS or 3) even GSLS
- Every architecture becomes an array of N*N zones (isochronous), so to multicores, massive parallelism, synchronization problems
- NoC: Network-on-Chip

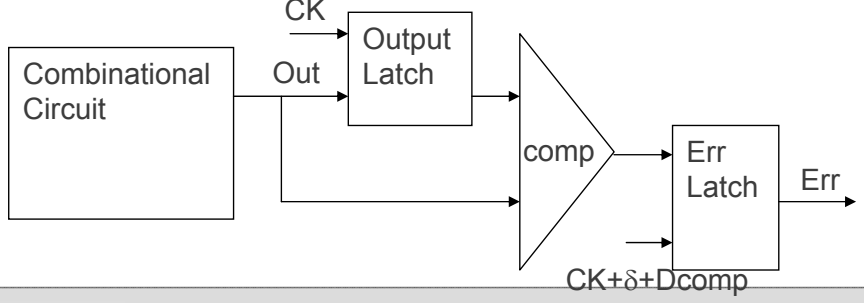


Example 3: Process Variations

- On the same die, technology variations from transistor to transistor (systematic, random), oxide thickness, W and L variations, doping, temperature and Vdd variations, even soft errors)
- VT Variations, factor 1.5 on delays and 20 on leakage
- Big impact on yield
- Which impact on architectures?
- For instance, to go for Multi-core, big parallelism. One can work at lower frequency for the same computation throughput. Consequently, the processor cores (at lower frequencies) are less sensitive to process variations on delay.
- Better to work at high Vdd (at low Vdd, 0.5 Volt, very sensitive to variations)
- Architectures with Fault-Tolerance, spatial or timing redundancy

Spatial or timing redundancy

- A system is not composed of reliable units, one has to consider that every unit could fail. However, the system could not fail!!
- A possible architecture is to use massive parallelism while presenting redundant units that could take over the work of faulty units.
- One can have spatial redundancy (very expensive) or timing redundancy (quite expensive in terms of throughput)
- And big problem, what about speed and power??
- To compare the result of a given operation at 2 different time frames
- RAZOR

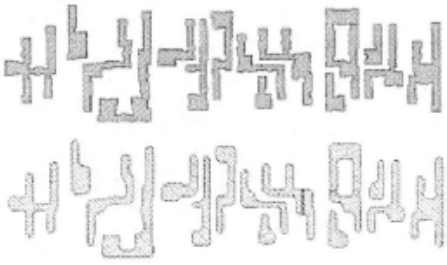


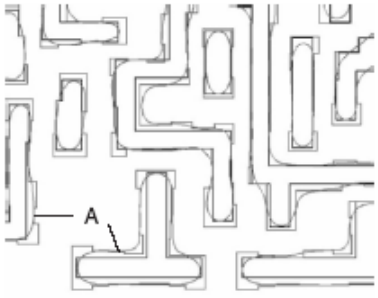
Subthreshold Logic

- Logic circuits based on transistors operated in weak inversion (also called subthreshold)
- This technique has been revived recently and applied to complete subsystems operated below 200 mV.
- It has been demonstrated that minimal energy circuits are circuits operated in subthreshold regime with Vdd reduced to under VT, resulting in lower frequencies and larger clock period.
- So dynamic power is reduced, static power is decreased, but the static energy is increased as more time is required to execute the logic function. So there is an optimum in energy.
- This optimal energy is also depending on logic depth and activity factor. The minimal Vdd (and minimal energy) is smaller for small logical depth and for large activity factors.

Example 4: Yield and DFM

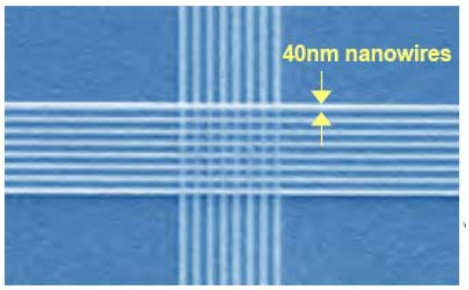
- DFM (Design For Manufacturing)
- Mask smallest dimensions are well below the lithographic light wavelengths.
- One has a lot of strange effects, bad line extension, missing small geometries, etc…
- To limit those variations by using regular layouts such as PLA or ROM for combinational circuits

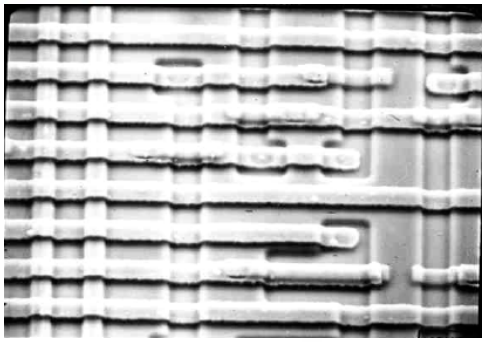




Impact of DFM on architectures

- Architectures based on regular blocks at layout level
- ROM, PLA, gate matrix, SoC fully dominated by memories

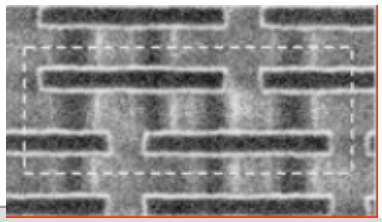




Gate matrix

8 x 8 crossbar switch built with 40nm nanowires

HP Labs – 2005



SRAM INTEL

Example 5: Alternative Energy Sources

- Many alternative and very diverse energy sources, with «energy scavenging»
  - batteries, fuel cells
  - Scavenging from environment, vibrations, thermoelectricity, solar cells, piezo, human energy sources, walking, shoes, mechanical watches
  - One has to generate inside the SoC multiples supply voltages with very diverse peak currents (some μA, some mA, up to 10 or 100 mA)
- « Power Management » circuits become very complicated (DC-DC, regulators).
- On top of this, one requires to add DVS and DVFS (Dynamic Voltage Frequency Scaling)

Impact of energy sources on architectures

- One has to manage these energy sources as well as DVFS, idle modes, recharge modes, etc…
- This can be performed by the Operating System, it is however quite complex
- This part of the embedded software has to interact with the application embedded software, that increases the overall complexity.

Increased Complexity

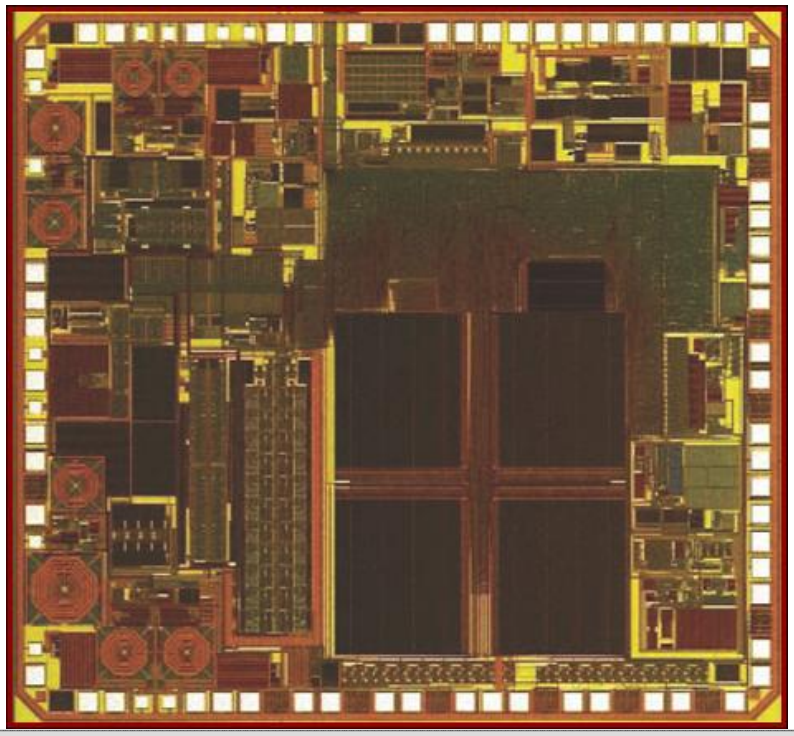
- More and more low level effects that have to be taken into account
- The impacts of these low level effects on to the high level synthesis process of MPSoCs is more and more difficult to understand and to take them into account
- Sure that only the low level effects have been presented here, but there are also effects at high level that have to be taken at low level:
    - Architecture for executing efficiently a given language
    - Asynchronous architecture requiring special standard cell library
    - Parallelizing compiler onto N processors, which are the constraints on to the processor architecture?

5. Heterogeneous MPSoC examples

- Wireless Sensor Network (Wisenet & Wisemac)
- BAW-based radios
- Vision sensor-based SoC
- Icyflex-based SoC
- OFDM Mobile TV chip

5.1 Wisenet SoC

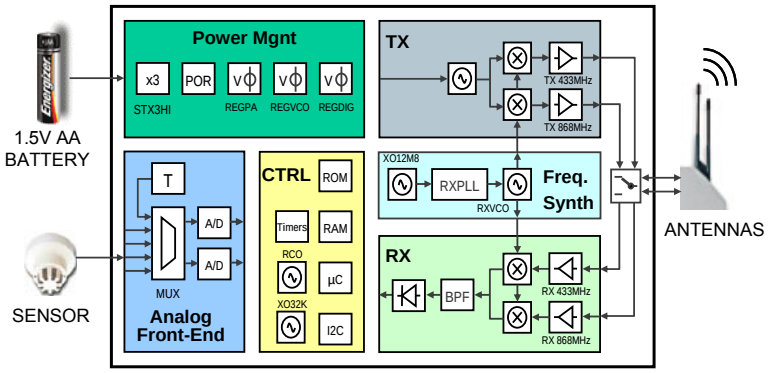
- Everything is low-power
- 400-800 MHz Radios
- 8-bit CoolRISC single core
- SRAM Memories
- Standard Cells
- A/D converters
- Sensors

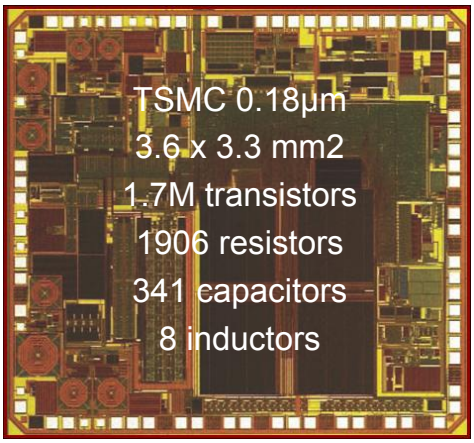


WiseNET SoC – first CSEM SoC (2004)

- 433MHz / 868MHz Rx & Tx
- CoolRISC µC with low leakage SRAM
- Analog sensor interface
  - 10-bit ADC
  - **4µA** Δ-Σ ADC with **10µV** resolution
- Power Management with step-up converters

- Low voltage SoC: **0.9V**-1.5V
- **I_{Rx}=2mA**, I_{Tx}=30mA @ 10dBm
- **I_{avg}=25µA** @ 0.1%-1.0% duty cycle
- 12.5-100kb/s in FSK, 2kb/s in OOK





Wisemac Protocol

- low power
- contention based
- uses preamble sampling
- minimize wake-up preamble length

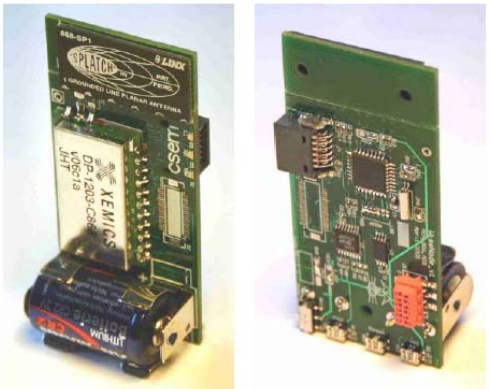
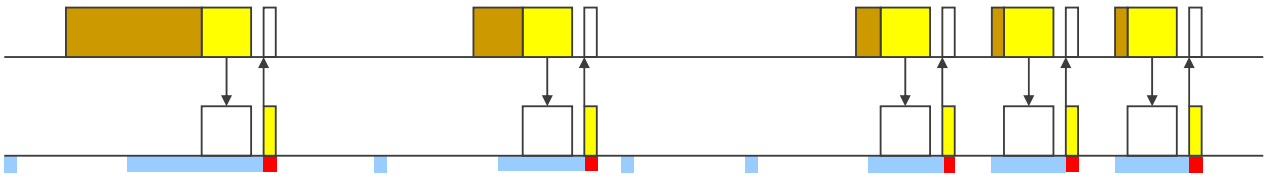
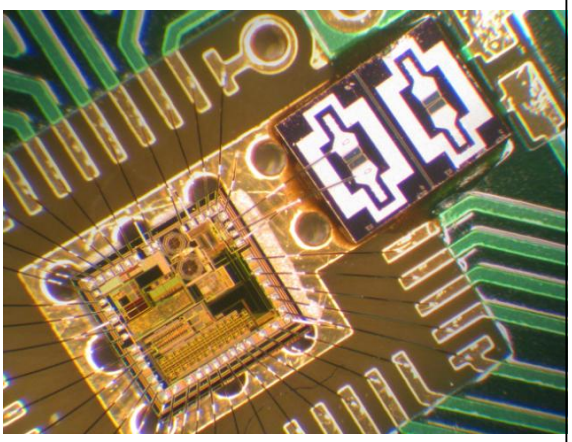


Figure 1. WiseNode Platform V1.0



5.2 RF-CMOS and BAW – A Real Opportunity

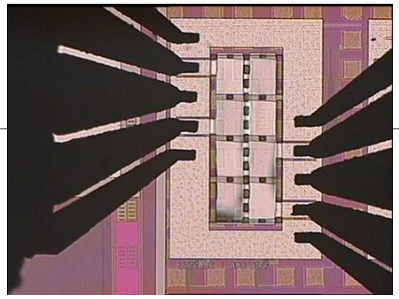
- Design of a new **ultra low-power** radio generation
- Use of **high-Q** BAW resonators
  - Performance: high quality factor **Q~1000**
  - Operation in RF within **1-10 GHz** range
  - Process steps **compatible** with **CMOS**
- Perspectives
  - Hi-Q allows reduced power (**autonomy**)
  - Higher performances (phase noise)
  - Co-integration with IC yields high degree of **miniaturization**



2.4 GHz RF-MEMS radio front-end

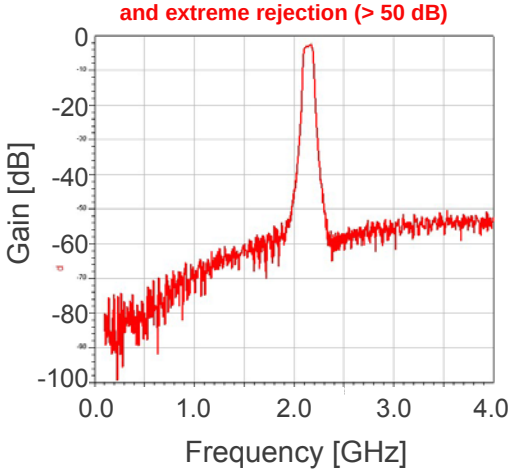
Bulk Acoustic Wave Devices

Differential filter under RF test

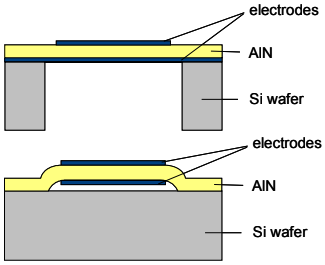


- Technology available for **FBAR** (membrane resonators) and **SMR** (resonators with acoustic reflector)
- Coupling coefficients up to 7%
- Design of single-ended or balanced filters

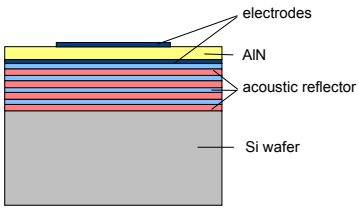
Differential response of filter with low loss and extreme rejection (> 50 dB)



FBAR

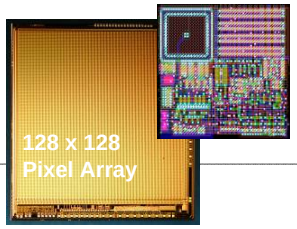


SMR



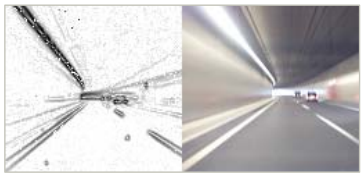
M.-A. Dubois *et al.* ISSCC 2005.

5.3 Vision sensors



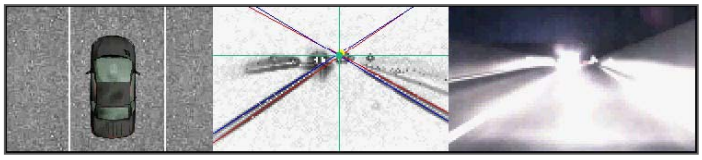
Extract **image features** from **contrast** magnitude and orientation and output **only** pixels with **pertinent** information

- Much **less data** to process
- **Real-time** operation, low-power and low-cost
- **Independent** of the **illumination** conditions
- Great **stability** (constancy) of representation
- Easy **motion** detection
- High dynamic range (**120dB**)



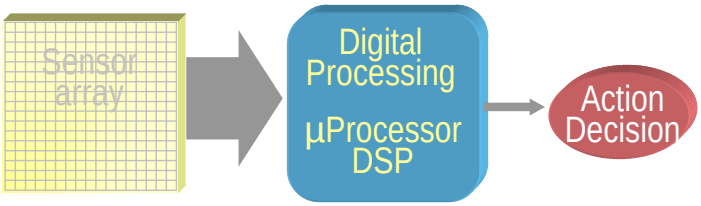
Automotive applications:

- **Lane departure warning**
- Collision warning
- Driver surveillance

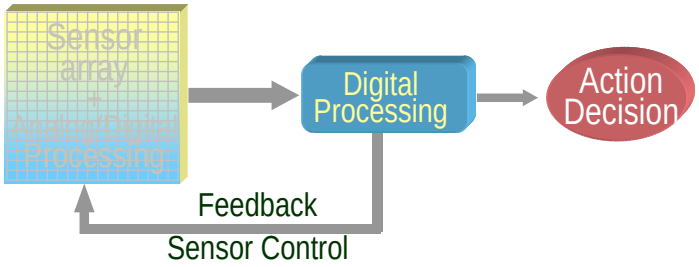


Sensory Information Processing: Vision Sensor

- Classical Approach
  - Imaging
  - ADC
  - « Number crunching »



- Our Approach
  - On-Chip Image Processing
  - light digital post-processing



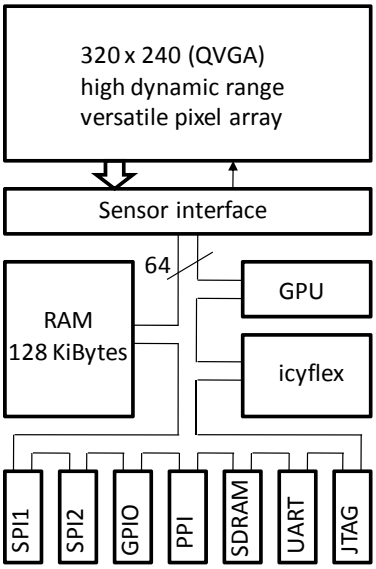
- Extraction & Processing of only sensor informations that are relevant for a given task

icycam, a SoC for Vision Applications

- Icycam is a circuit combining on the same chip a 32-bit icyflex processor operated at 50 MHz, and a high dynamic range versatile pixel array, integrated on a 0.18 µm optical process.

-The pixel array has a resolution of 320 by 240 pixels , with a pixel pitch of 14 um.

- Able to extract on the fly the local contrast magnitude (relative change of illumination between neighbour pixels) and direction when data are transferred from the pixel array to the memory



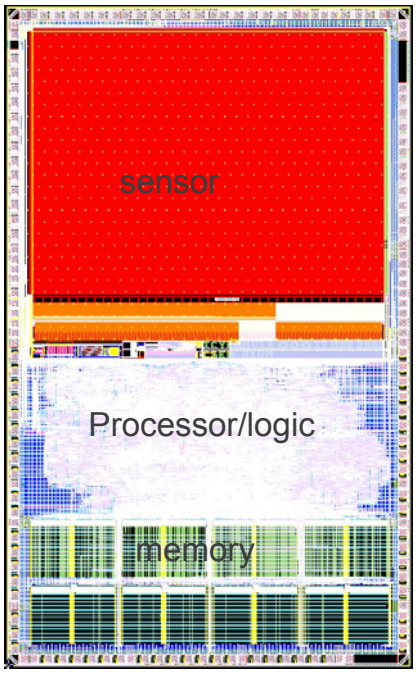
MPSoC with local pixel processing and icyflex

- Data transfer between the pixel array and memory or peripherals is performed by group of 4 (10 bits per pixel) or 8 (8 bits per pixel) pixels in parallel at system clock rate.

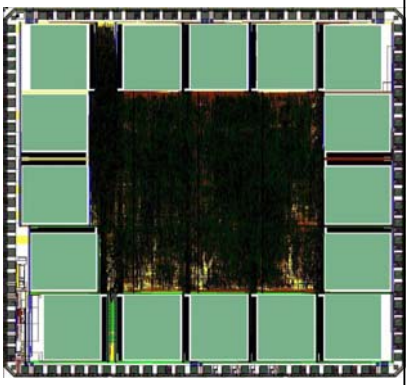
-These image data can be processed with the icyflex's Data Processing Unit (DPU) which has been complemented with a Graphical Processing Unit (GPU) tailored for vision algorithms, able to perform simple arithmetical operations on 8- or 16-bit data grouped in a 64-bit word.

- Internal SRAM being size consuming, the internal data and program memory space is limited to 128 KiBytes. This memory range can be extended with an external SDRAM up to 32 MiBytes.

- 43 mm2



5.4 Icy*flex*: 32-bit microcontroller and 2//MAC DSP core

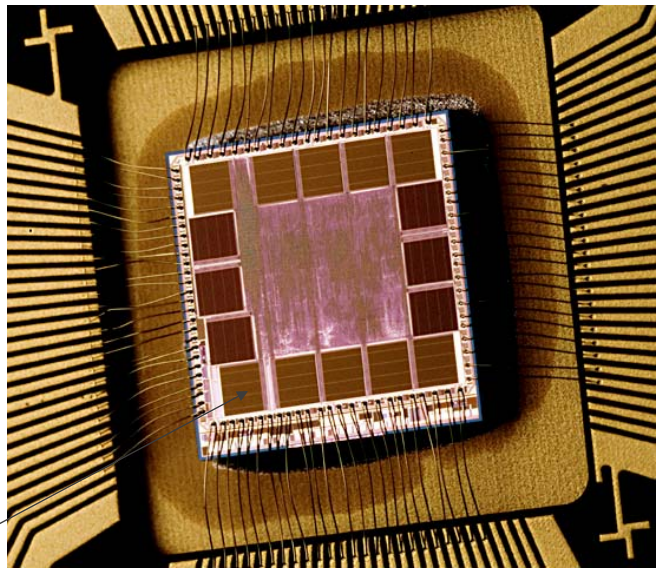


Development of the **icy*flex*** replacing the 8-bit CoolRISC for integration in future CSEM SoCs

- 32-bit **customizable** and **configurable** multi-purpose processor
- for **digital signal processing**, includes 2 multiply – accumulate MAC units
- for less regular control logic (supports a C compiler)
- **ultra low power** consumption (120µW/MHz at 1V)
- **first silicon** (Nov 2006) is functional
- software development tool chain based on GNU tools (gcc C compiler, gas assembler, gdb debugger)

Icy*flex*-based SoC (Nov. 2006)

- This integration targets **very low leakage** for applications requiring limited processing power
- Standard cell library: **thick gates**
- Leakage reduction by 800x
- Measured speed: 400 kHz @ 1.1 V
- Avg dyn power: 120 µW/MHz @ 1.0 V
- Core: 115k eq. gates, 1.75 mm^2
- Peripherals: 110k eq. gates, 1.5 mm^2
- Memory: 10.7 mm^2
- Process: TMSC 180 nm



Performance: Comparison with other DSPs

Company / Processor	FIR filter Clock cycles per tap	Complex FFT 256 points Clock cycles
CSEM / Macgic	~1/4	1.5k
CSEM / icyflex	~1/2	2.6k
Analog Devices / Blackfin BF531	~1/2	3.2k
Texas Instruments / TMS320VC5501	~1/2	5.5k
Philips / CoolFlux DSP	~1/2	5.5k
Analog Devices / ADSP2191M	~1	7.4k
Motorola / M56F8323	~1	12k
MicroChip / dsPIC30	~1	~19k
Texas Instruments / TMS320F2810	~1/2	25k
Texas Instruments / MSP430F14x	~28	~53k
MicroChip / PIC18F4220	~160	3.2M

Comparison of Starcore, CoolFlux, Macgic and icyflex

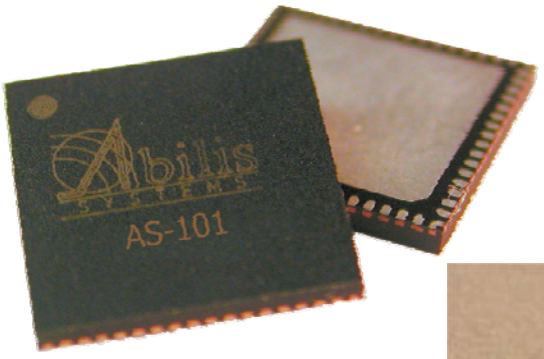
Features	Starcore	Macgic	icyflex	CoolFlux
Bits per Instruction	128-bit	32-bit	32-bit	32-bit
Data Word width	16-bit	32/24-bit	32-bit	24-bit
Number of MAC	4	4	2	2
Memory Transfer	8	8	4	2
Operations per cycle	32	32	16	8
Number of equivalent NAND gates	600k	150k	110k	45k
Clock cycles for FFT 256	** 1'614	1'410	2'700	* 5'500
Average Power per MHz @ 1V	* 350 µW	170 µW	*120 µW	* 75 µW
Power per MHz @ 1V for FFT	* 600 µW	300 µW	*215 µW	* 130 µW
Normalized energy for FFT @ 1V	2.3	1	1.4	1.7

**single precision *estimated

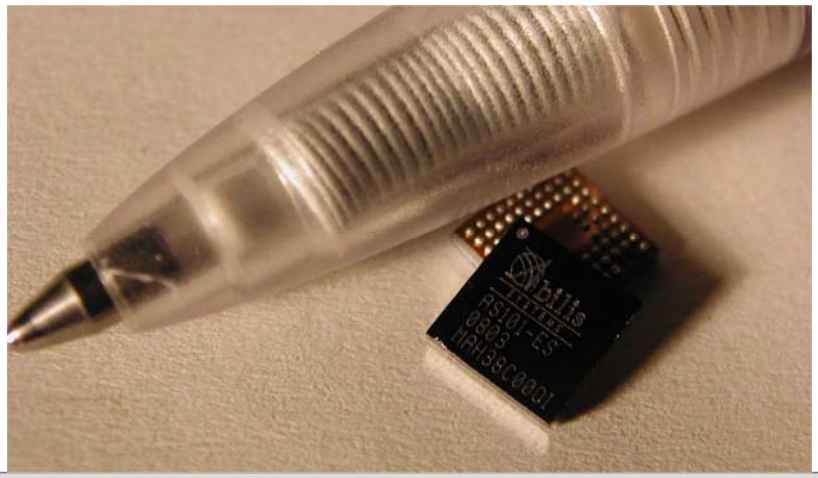
Audio-I Test Chip Characteristics

- Technology: TSMC 0.18 µm
- Integration date: March 2005
- Size: 3.6 mm by 5.0 mm = 18 mm²
- Gates: 200'000 (excluding the RAMs)
- Standard cell lib: CSEM's CSL 6.0 for low power consumption
- Memory: 96 KBytes of CSEM's low power RAM
- Signal pads: 50 (HDU ports are not available as pads)
- Voltage RAM/core: 0.9V to 1.8V
- Voltage pads: VDDcore to 3.3V
- Frequency: 7 MHz @0.7V; 35MHz @1V; 80 MHz @1.8V
- Power consumption: 72 µW/MHz @0.7V; 150 µW/MHz @ 1V

5.5 Mobile TV Chip (DVB-T/H) by Abilis

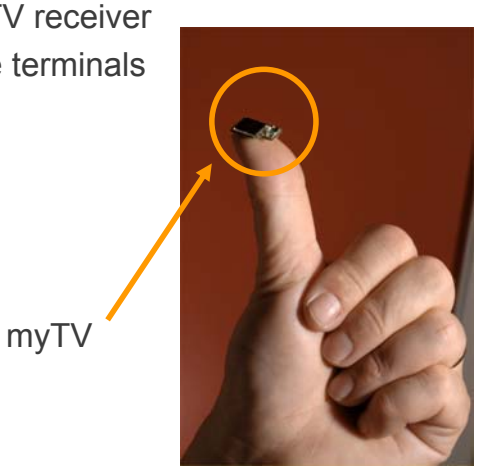


Abilis SYSTEMS



This chip contains three MACGIC cores

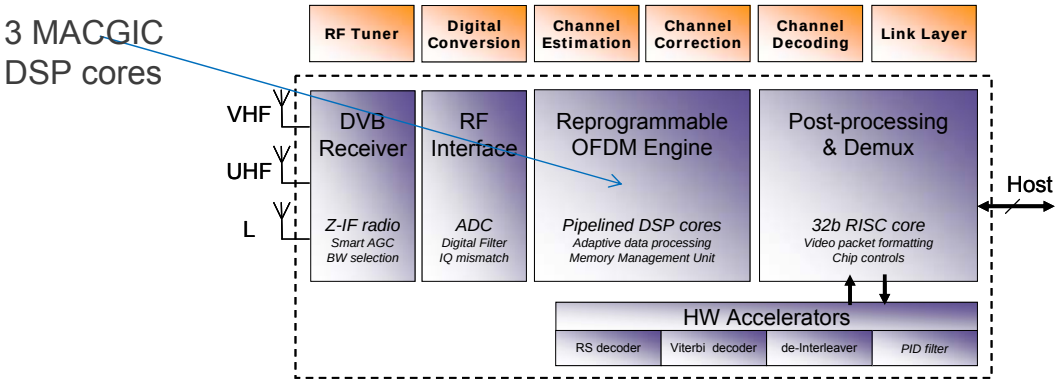
- **Abilis:** To become the world leading supplier of semiconductor solutions of multimode, digital TV receiver and broadband wireless connectivity for mobile terminals



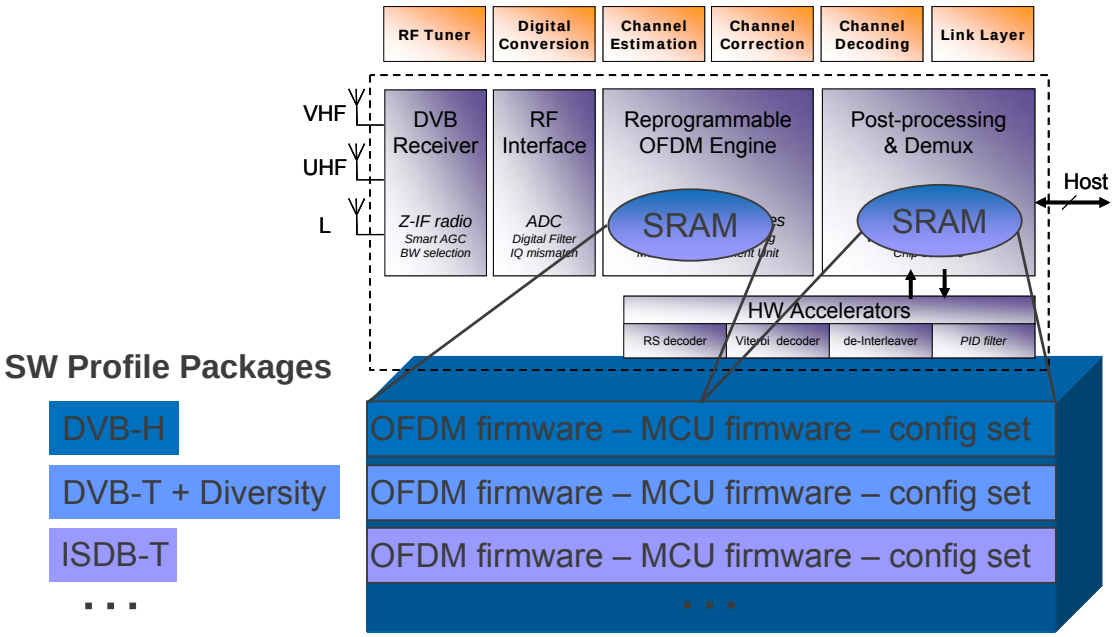
Abilis Technology

- Low Power Software Define Radio (OFDM Engine)
- Multi modes System Partitioning

- **Quad-band, Low Power RF**
- **IBM CMOS 90nm technology**



Multi Standard Software Profiles

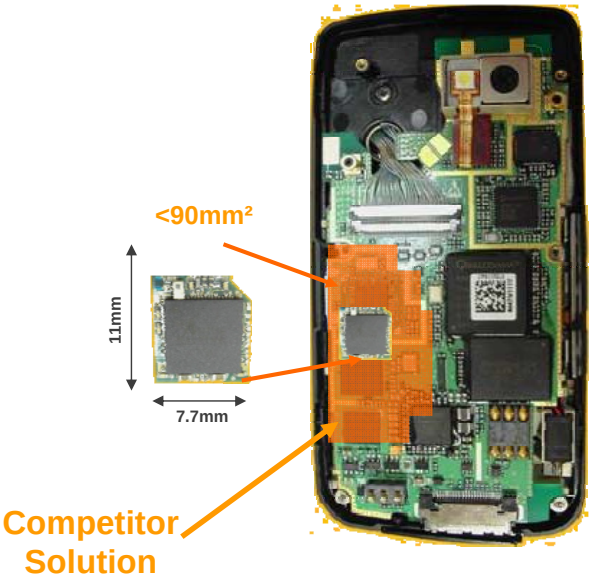


AS-101 Mobile TV Phone

- **Smaller than <90mm²**
  - Actual Size is 7.7mm / 11.7mm
    - CSP package
    - <20 external components: <20¢
      - 1 Balun, decoupling caps
    - One frequency band
  - External crystal re-use
  - SPI interface
  - 1.2V and 2.5V supply

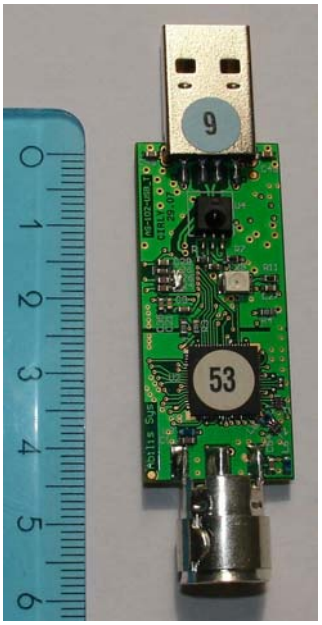
- **Pre-certified System Solution**
  - HW design
  - Partnership with ESG/EPG middleware suppliers
  - SW Driver Source Code

Major Area/Cost Reduction



AS-102 DVB-T PC TV

- **Highly Integrated Solution**
  - Multi-band tuner
  - Advanced demodulator
  - USB 2.0 interface
  - QFN 9mm x 9mm
  - Power dissipation < 350mW
- **Very Efficient BOM**
  - Low external component count
  - 1 Balun, decoupling caps
  - Single crystal solution
  - On board USB PHY interface
- **Pre-Certified System Solution**
  - HW design
  - Partnership with ESG/EPG middleware suppliers
  - SW Driver Source Code



6. « Disruptive » Architectures and Systems??

- One can look at various Roadmaps
- The end of CMOS «scaling» is predicted around 11 nanometers, roughly 10 years from now, around 2013 and 2017
- After 2017, we should move to « Beyond CMOS »
- However, today, there is no clear alternating route to replace CMOS
- CNT, nanowires, molecular switches etc… it is not so clear for architectures and systems requiring billions of switches and billions of wires or interconnect
- Nevertheless, there is an interesting approach in hybrids CMOS and nano, it will be heterogeneous…
- With these nano-elements, one has sometimes the same problems at low level (leakage, process variations), but we could also imagine or hope that some of these effects would disappear!!

However, one can take some risk by having new ideas..

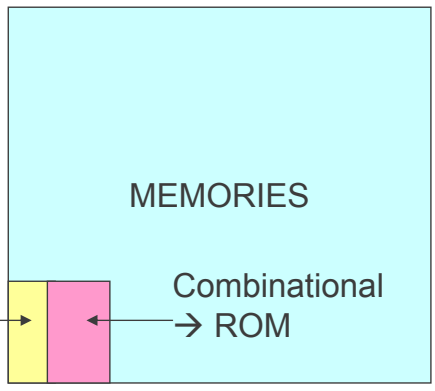
- **A single universal SoC or MPSoC platform:** everybody has to use the same hardware, consequently, design is fully concentrated on embedded software.
  - Very expensive to develop, about 100 M€, and one could ask if is reasonable for applications sensitive to power consumption and to some other performances…
- A **SoC or MPSoC dominated by memories**

Memories are automatically generated, so the hardware part to design is very small.

But one re-generates only the used memories…

Less wasted silicon

This is very small (?) → Execution Radio Peripherals



And still new Architectures…

- **SoC or MPSoC with 1'000 parallel processors** « A View of Berkeley »
  - Not the same than multicore (2 à 32)
  - Small logic blocks of 50K gates, and… a lot of memory…
- **Architecture with nano-elements**
  - Completely different, bottom-up design methodology (not top-down)
  - Sure very and very regular circuits and layouts
  - Applications which will be completely different than Pentium
- **Other idea?**

7. Conclusion

- Diagnostic is clear:
  - Complexity increases, interdisciplinary too
  - More and more interactions between all design levels
  - We are going higher and higher (ARTEMIS) but also lower and lower (ENIAC), resulting in a gap which increases
  - We see design teams that are also more and more heterogeneous
- What we have to do is also more difficult to define:
  - Focused research, yes, but primarily interdisciplinary research
  - To talk to many people, to understand more and more people
  - To go to conferences…

Tank you for your attention.

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